In the Claims:

1-24. (canceled)

25. (previously added)A process of operating an integrated circuit, comprising:

A. scanning a first signal into a serial scan path on the integrated circuit in response to a scan clock signal and a scan mode signal;

B. storing the first signal in a register on the integrated circuit, the register being coupled to the scan path on the integrated circuit, the first signal indicating a desired protocol;

C. operating functional circuits on the integrated circuit to produce operating signals;

D. comparing, on the integrated circuit, the operating signals to compare signals stored in an expected data memory, on the integrated circuit;

E. generating an event signal, on the integrated circuit, when the operating signals match the compare signals; and

F. in response to the event signal, performing a circuit operation on the integrated circuit using the desired protocol.

26. (previously added)The process of claim 25 in which the operating includes producing operating signals on at least one bus of operating signal leads, and the comparing includes comparing the operating signals on the at least one bus of operating signal leads to the compare signals.

27. (previously added)The process of claim 25 in which the storing includes storing the first signal in a register of the scan path.

28. (previously added)The process of claim 25 in which the scanning includes scanning a first signal from a scan data input on the integrated circuit to one of plural scan paths on the integrated circuit.

29. (previously added)The process of claim 25 including scanning a second signal into the serial scan path on the integrated circuit in response to the scan clock signal and the scan mode signal, and storing the second signal in a second register coupled to the scan path on the integrated circuit, the first and second signals indicating the desired protocol.

30. (previously added)The process of claim 25 in which the performing includes performing a data sample protocol.

31. (previously added)The process of claim 25 in which the performing includes storing operating signals in a data sample register.

32. (previously added)The process of claim 25 in which the performing includes storing operating signals in a data sample register and scanning the stored data out of the data sample register on a scan path that is coupled to the data sample register.

33. (previously added)The process of claim 25 in which the performing includes storing operating signals in a data sample register and scanning the stored data out of the data sample register on a scan path that extends into and out of the data sample register.

34. (amended)The process of claim 25 in which the performing includes: storing operating signals in a data sample register, and scanning the stored data out of the data sample register on a scan path that is coupled to the

data sample register, and that extends to a scan data output on the integrated circuit.

35. (previously added) The process of claim 25 including scanning a third signal into the serial scan path in the integrated circuit in response to the scan clock signal and the scan mode signal, the third signal being an enable signal, and the performing including performing a circuit operation on the integrated circuit using the desired protocol in response to the event signal and the enable signal.

36. (previously added) The process of claim 25 including scanning a third signal into the serial scan path in the integrated circuit in response to the scan clock signal and the scan mode signal, the third signal being an enable signal, storing the third signal in a third register coupled to the scan path on the integrated circuit, and the performing including performing a circuit operation on the integrated circuit using the desired protocol in response to the event signal and the enable signal.

37. (previously added) The process of claim 25 including generating the event signal in response to an event occurring external of the integrated circuit.

38. (previously added) The process of claim 25 including detecting a fourth signal on the integrated circuit, the fourth signal indicating the end of the operation of the desired protocol.

39. (previously added) The process of claim 25 in which the performing includes inputting signals to a serial data register from an operating bus in the integrated circuit.

40. (previously added) The process of claim 39 including serially scanning the input signals from the serial data register after the inputting signals to a serial data register.

41. (previously added)A process of operating an integrated circuit, comprising:

A. scanning a first signal into a serial scan path on the integrated circuit in response to a scan clock signal and a scan mode signal;

B. storing the first signal in a register on the integrated circuit, the first signal indicating a desired protocol;

C. detecting an event signal; and

D. in response to the event signal, performing an operation on the integrated circuit using the desired protocol.

42. (previously added)The process of claim 41 in which the storing includes storing the first signal in a register of the scan path.

43. (previously added)The process of claim 41 in which the scanning includes scanning a first signal from a scan data input on the integrated circuit to one of plural scan paths on the integrated circuit.

44. (previously added)The process of claim 41 including scanning a second signal into the serial scan path on the integrated circuit in response to the scan clock signal and the scan mode signal, storing the second signal in a second register coupled to the scan path on the integrated circuit, the first and second signals indicating a desired protocol.

45. (previously added)The process of claim 41 in which the performing includes performing a data sample protocol.

46. (previously added)The process of claim 41 in which the performing includes storing operating signals of functional circuits in a data sample register.

47. (previously added)The process of claim 41 in which the performing includes storing operating signals of functional circuits in a data sample register and scanning the stored data out of the data sample register on a scan path that is coupled to the data sample register.

48. (previously added)The process of claim 41 in which the performing includes storing operating signals of functional circuits in a data sample register and scanning the stored data out of the data sample register on a scan path that extends into and out of the data sample register.

49. (amended)The process of claim 41 in which the performing includes: storing operating signals of functional circuits in a data sample register, and scanning the stored data out of the data sample register on a scan path that is coupled to the data sample register, and that extends to a scan data output on the integrated circuit.

50. (previously added)The process of claim 41 including scanning a third signal into the serial scan path in the integrated circuit in response to the scan clock signal and the scan mode signal, the third signal being an enable signal, and the performing including performing a circuit operation on the integrated circuit using the desired protocol in response to the event signal and the enable signal.

51. (previously added)The process of claim 41 including scanning a third signal into the serial scan path in the integrated circuit in response to the scan clock signal and the scan mode signal, the third signal being an enable signal, storing the third signal in a third register coupled to the scan path on the integrated circuit, and the performing including performing a circuit operation on the

integrated circuit using the desired protocol in response to the event signal and the enable signal.

52. (previously added)The process of claim 41 including generating the event signal in response to an event occurring external of the integrated circuit.

53. (previously added)The process of claim 41 including generating the event signal in response to an event occurring on the integrated circuit.

54. (previously added)The process of claim 41 including detecting a fourth signal on the integrated circuit, the fourth signal indicating the end of the operation using the desired protocol.

55. (previously added)The process of claim 41 in which the performing includes inputting signals to a serial data register from an operating bus in the integrated circuit.

56. (previously added)The process of claim 55 including serially scanning the input signals from the serial data register after the inputting signals from a serial data register.